(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 632 685 A2**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **94108592.0**

(51) Int. Cl.[6]: **H05K 7/20**, H05K 1/00

(22) Date of filing: **01.06.94**

(30) Priority: **03.06.93 US 71630**

(43) Date of publication of application:
04.01.95 Bulletin 95/01

(84) Designated Contracting States:
DE FR GB

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(54) **Flexible circuit board assembly with common heat spreader and method of manufacture.**

(57) Disclosed are multi-layer substrates for flexible circuit boards and flexible circuit board assemblies and their methods of manufacture.

More particularly multi-layer flexible circuit board substrates are described for attaching components including chips and heat spreaders to form a three-dimensional circuit board assembly.

EP 0 632 685 A2

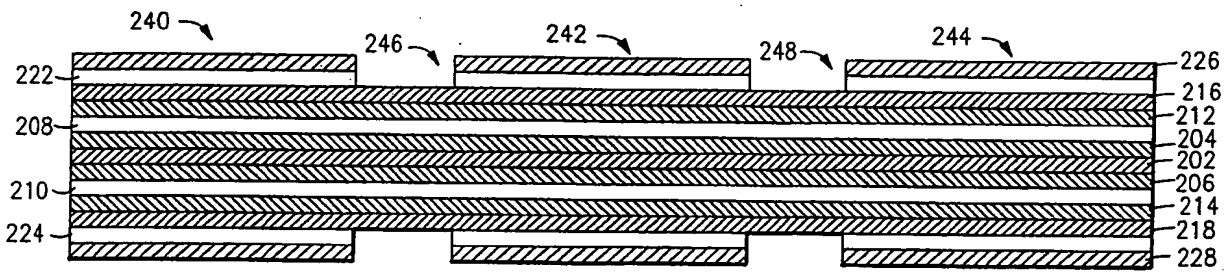

FIG.2

FIELD OF INVENTION

The present invention relates to multi-layer substrates for flexible circuit boards and flexible circuit board assemblies and their methods of manufacture. More particularly this invention relates to a multi-layer flexible circuit board substrate for attaching components including chips and heat spreaders to form a three-dimensional circuit board assembly.

BACKGROUND

All levels of packaging, (chip, electronic circuit assembly and systems are becoming more) miniturizated. A major technical challenge is thermal dissipation as power density increases. Typically heat spreaders or heat sinks are bonded to microelectronic components and chips, individually. Occasionally, a common heat sink may be bonded to multiple chips on co-planer top surfaces. In many applications, space limitations and cost do not allow the use of heat sinks or planer electronic assemblies.

Flexible circuit boards offer advantages of light weight, thinness, three dimensional configuration, and flexibility. Space and height constraints for circuit packaging may dictate the use of flexible circuits over rigid laminates and very low profile chips and packages over high profile chip modules.

US-A-3,781,596 discloses a single layer interconnection structure of metallic conductors on a polyimide film (e.g. KAPTON™ by E.I. DuPont de Nemours). US-A-3,868,724 discloses metallic conductors sandwiched between polyimide film which project through the film.

Rigid-Flex circuit boards are described in US-A-5,121,297 to Haas and US-A-5,144,742 to Lucas. In those patents single layer flex circuit boards are integrally connected between rigid circuit boards. In both patents multiple rigid circuit board layers are laminated to a flexible circuit board substrate and components are attached only onto the rigid circuit board sections.

Connecting components directly to one side of a single-layer flexible circuit board is described by McBride, "Multi-function Plug for IC Package", IBM Technical Disclosure Bulletin Vol. 21, Feb. 1979, pp. 3594-3595. I/O terminals on the bottom of a chip are soldered to pads on top of a thin polyimide flexible decal. Also, a depression in a heat sink cover is bonded onto the top of the chip. Connecting lower power chips to a bottom side of a multi-layer flexible circuit board and high power chips to the top side of the flexible circuit board in order to connect the high power chips to the module cap is suggested by McBride, "Multilayer Flexible Film Module", IBM Technical Disclosure Bulletin Vol. 26, May 1984, p. 6637. In that article I/O pins connect the flexible film to a metalized ceramic substrate, and smaller pins interconnect the layers of the film. Schrottke, "Removal of Heat from Direct Chip Attach Circuitry", IBM Technical Disclosure Bulletin Vol. 32, Sept. 1989, pp. 346-348 describes a flexible circuit board with two rows of Direct Chip Attach (DCA) chips attached by controlled collapse chip connections (C4). The flexible circuit board is folded around a stiff heat spreader of copper-INVAR-copper (INVAR is a trademark of Creusot-Loire for a nickel-iron alloy) with the chips on the inside of the fold. The exposed surfaces of each row of chips are bonded with a thermally conductive adhesive to a respective major surface of the spreader.

US-A-5,179,501 to Ocken, and US-A-5,159,751 to Cottingham disclose bonding flexible circuit boards directly to one side of an aluminum plate. In Ocken, heat is conducted through the circuit board to a first heat sink plate then to a second heat sink plate bonded to the first plate. "Concept for Forming Multilayer Structures for Electronic Packaging" (Curtis), IBM Technical Disclosure Bulletin Vol. 30, Aug. 1987, pp. 1353-1356 and U.S. patent 4,811,165 to Currier, disclose folding a flexible circuit board around a heat sink plate and bonding the board to both sides of the plate. In both citations, before bonding the board to the plate, components are connected to the side of the board which is not connected to the plate. "Integral Heatsink Printed Circuit Board" (Askalv), IBM Technical Disclosure Bulletin Vol. 25, Dec. 1982 p. 3606, discloses a flexible circuit board adhesively bonded to a heat sink of steel or aluminum.

US-A-5,168,430, discloses a portion of a flexible circuit board applied to a heat sink plate and provided with a cutout in which a hybrid circuit structure is cemented to the plate. The hybrid circuit structure is wirebonded to the flexible circuit board.

US-A-4,834,660 to Cottiat, Figure 9 shows a circuit board interconnection system in which layers of a flexible circuit board are removed in part of a bend to expose a selected wiring layer for connection. The flexible circuit board is of copper clad polyimide.

All the above citations are hereby incorporated by reference.

OBJECTS OF THE INVENTION

A general object of the invention is to provide an improved flexible circuit board substrate.

Another object of the invention is to provide enhanced thermal operation of flexible circuit boards with components mounted to both sides.

Another object of the invention is to provide a method and apparatus to produce a flexible circuit board with components mounted on screened paste on both sides of the circuit board. Components include wire bond, flip chips, SM (Surface mount) active discreates, and PIH (pin-in-hole).

A further object of the invention is to provide an improved heat sink structure for flexible circuit boards.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a process flow diagram of a specific embodiment of the process for forming a circuit board substrate of the invention;

FIG. 2 is a schematic cross section of a specific embodiment of the circuit board substrate of the invention showing the layers of the thicker, stiffer areas and thinner, more flexible areas;

FIG. 3 is a schematic cross section of a part of the embodiment of FIG. 2 showing the plated through holes and windows in the stiffer areas;

FIG. 4 is a process flow diagram of a specific embodiment of the initial process for mounting components to the front side of the substrate of the invention to form a circuit board of the invention;

FIG. 5 is plan view of a specific embodiment of the back side of the circuit board of the invention;

FIG. 6 is an elevation of the circuit board of FIG. 5 showing the heat sinks on the front side;

FIG. 7 is a plan view of a section of the front of the circuit board of FIG. 5 with the heat sink plates removed and with some other components also removed for illustration;

FIG. 8 is a plan view of the back side of the same section of the circuit board as in FIG. 7 with some components removed for illustration;

FIG. 9 is a schematic plan view of a specific embodiment of the fixture of the invention for holding the circuit board front side down for screening paste on the back side;

FIG. 10 is a partial cross section of a part of the back plate of the fixture of FIG. 9 through section lines 10-10 showing the cavities conforming to components mounted on the front side of the circuit board;

FIG. 11 is a process flow diagram of a specific embodiment of the process for mounting components onto the back side of the circuit board of the invention;

FIG. 12 is a process flow diagram of the process for mounting flip chips to solder bumps on the front side of the circuit board of the invention;

FIG. 13 is a process flow diagram for a specific embodiment of the method of bonding the circuit board, flip and wirebond chips to the heat sink plate and encapsulating the wirebond chips in the invention;

FIG. 14 is a schematic cross section showing part of the connections between the heat sink, flexible circuit board, flip chips, wirebond chips and SMT (surface mount technology) chips connected to the circuit board in a specific embodiment of the invention;

FIG. 15 is a process flow diagram for finishing up the circuit board of the invention;

FIG. 16 is a cross section of the three heat sink plates attached to an enclosing frame and showing the attached circuit board in a specific embodiment of the invention;

FIG. 17 is an end view of heat a sink plate in a psecific embodiment of the invention.

ENABLING DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1 illustrates a specific example of the process 100 for producing the circuit board structure of the invention and FIG.s 2 and 3 schematically illustrate an example structure of the circuit board substrate 200 of the invention with thickness exaggerated for clarity. In step 102 of FIG. 1, the base substrate may be formed (see FIG. 2) by covering both major surfaces of a dielectric film 202 with a respective layer of adhesive 204, 206. Preferably, the dielectric layers of the base substrate are dry polyimide film such as KAPTON by DuPont and the adhesive layers are a dry epoxy film and both the dry polyimide film and film adhesive used in this process are about 0.025 mm thick. Then the exterior surface of each film adhesive layer is covered with a patterned metal layer 208, 210 resulting in a two layer circuit board. Preferably the metal layers are copper foil which are previously etched to form a circuit pattern and are about 0.018 mm thick and include a chromium layer deposited on both major surfaces of the copper foil to avoid oxidizing the copper and to promote adhesion. Then the exterior surface of each patterned copper foil is covered with another layer of adhesive 212, 214 and then another layer of dielectric 216, 218 as described above. Then the entire structure is laminated under heat and pressure. Other processes for making such a two layered flexible circuit board base with external dielectic coverings are well known in the art.

In step 104, via holes 232, 234 are formed through the circuit board by for example punching or drilling, and are preferably 0.01 - 0.04 mm across and more preferably about 0.025 mm across. Additional holes 236, 238 may be similarly formed through the circuit board for other purposes such as attaching pin-in-hole (PIH) components and connectors and the diameters of such addi-

tional holes will depend upon their use.

In step 106, a deposited metal wiring layers 222, 224 are formed. Metal is deposited in the through holes 223, 234, 236, 238 and on the exterior surfaces of the outer dielectric layers 216, 218. Preferably, the metal is electroplated or electrolessly plated and about 0.025 mm thick on the surface using a photo-chemical additive or more preferably a subtractive photo-chemical process to pattern the copper. In step 106, each deposited copper pattern is covered with an additional dielectric layer 226, 228 such as a solder resist. Preferably the solder resist is Taiyo (PSR 4000®).

The holes, additional deposited copper layers, and additional dielectric layers of steps 102 through 104 are provided only at selected parts of the exterior of the circuit board to define thicker, stiffer areas 240, 242, 244 where additional wiring and dielectric layers extend and to define more flexible, thinner areas 246, 248 through which the circuit board can be bent about a line without bending the stiffer areas. The additional wiring patterns may include connection pads 250, 252 for leaded surface mount technology (SMT) components, wirebond pads 254, 256 for wirebond chips and arrays of pads 258, 260 for soldered flip chip interconnection. Pads may include vias such as 232, 234 as shown in FIG. 3.

In step 110, rectangular windows 270 shown in FIG. 3, may be punched, drilled or otherwise formed by known processes through the circuit board for any wirebond chips which need to be bonded to a heat sink attached to the circuit board. The windows will typically be surrounded by rows of wirebond connection pads 254, 256 forming a rectangle around the windows.

The description of the formation of the substrate is complete and components need to be added to form a circuit board.

FIG. 4 illustrates a specific embodiment of the process 300 of the invention for attaching components to the front of the substrate for producing a specific circuit board embodiment 400 of the invention illustrated in FIGs 5 through 8.

In step 302, solder paste may be screened through a mask onto pads 402, 404, 406, 408 for attaching leads of Surface Mount Technology (SMT) components on a front side of the circuit board as best seen in FIG. 7. Preferably, a water clean paste is utilized such as ALPHA 1208® (of Alpha Metals) and more preferably a no-clean paste such as ALPHA LR701® or even more preferably KESTER R-244®. Then in step 304, SMT components 410 are positioned with leads on the paste on the SMT pads on the front side of the circuit board. If area array direct chip attachment is required, solder may need to be applied to pad arrays. One method of applying such solder is by transferring from solder preform decals by reflow. Flux is applied to solder preform decals 411 in step 306 and is preferably a no-clean flux. The preform decals are aligned and placed onto flip chip pad arrays 412 on the front side of the circuit board in step 308. Alternatively, solder may be applied to the board chemically, or electrically, or by wave solder; or eutectic solder may be applied to the high temperature solder balls on the flip chip.

In step 310, the circuit board is heated sufficiently to reflow the paste to solder the SMT components to the SMT pads and transfer the solder of the preforms from the decals to the pad arrays to form solder bumps. Preferably, reflow is by infrared heating in an oven with an N_2 atmosphere and preferably the heating profile consists of a ramp up of about 1.8 degrees C/sec, Dwell at about 150 to 160 degrees C for about 200 to 250 seconds and at about 180 degrees for about 90 to 145 seconds. Finally in step 312, after any solder decals are removed from the circuit board, the SMT connections and flip chip site solder bumps are visually inspected preferably with a microscope and touched up by adding any additional solder volumes required and locally reflowing the added solder as needed. The solder is preferably added by manually applying solder preforms to the pads or connections. If water clean pastes or fluxes have been applied, then the circuit board should be cleaned with de-ionized water.

FIG's 9 and 10 illustrate the fixture 500 for holding the flexible circuit board 502.

FIG. 11 illustrates a specific embodiment of the process 700 of the invention for attaching components to the back of the substrate to produce a specific circuit board embodiment 800 of the invention illustrated in FIG. 8.

In step 702, circuit board 400 is placed in a holding fixture 500 with the front side of the circuit board facing down onto back plate 504 with cavities 506, 508 conforming to components 510, 512 mounted on the front side of the circuit board. Stretching clamps 514 through 520 pull the corners of the board with approximately equal force in approximately diagonal directions as represented by equal sized arrows 522 through 528.

In step 704, solder paste is screened through another mask onto pads 802, 804 for attaching Surface Mount Technology (SMT) component 806 and screened onto plated through holes 808, 810 for attaching pin-in-hole (PIH) components 812 on a back side of the circuit board (see FIG. 8). Again no-clean solder pastes described above are preferred. Components 806, 812 are placed on the paste on the pads on the back side of the circuit board in step 706. In step 708, the circuit board is heated for a second reflow for soldering the SMT and PIH components to the back side of the circuit

board. Preferably, the reflow temperature profile is similar to the profile for the first circuit board reflow and again infrared heating is preferred. Finally the circuit board is removed from fixture 500 in step 710. Alternately, the circuit board may be removed from the fixture any time after screening. If only PIH components are to be placed, then molten solder wave may be substituted for the above screening and reflowing procedure.

FIG. 12 illustrates the process 900 for attaching and encapsulating flip chip 414 on the front of circuit board 400 as shown in FIG 4. In step 902, the area arrays of solder bumps 412 on the front side of the circuit board are mechanically flattened, preferably using a semi-automatic pneumatic bump flattener. In step 904, flux is applied to the flip chips and/or to the arrays of solder bumps. Preferably, the flux is a no-clean flux described above. The flip chips are aligned and placed on the flattened solder bump area arrays on the front side of the circuit board in step 906.

In step 908, the circuit board receives a third reflow heating cycle preferably in a reflow oven for flip chip connection to the front side of the circuit board. Preferably, the reflow temperature profile melts the eutectic solder connection between the high temperature solder ball and the chip pad in order to let the solder ball float to a position intermediate between the chip pad and circuit board pad or via to minimize stresses.

In step 910, the circuit board is tested and chips are reworked as required to meet electrical specifications. If required, the circuit board is baked in step 912 to drive off any water or other solvents. Preferably, the board is baked at about 112 degrees centigrade for about 2 hours. In step 914, liquid plastic encapsulant, preferably HYSOL FP4511®, is dispensed to fill the space under the flip chips. Preferably, any SMT and PIH components are also encapsulated. Then the encapsulant is cured in step 916, preferably in an oven and at about 130 degrees centigrade and for about 5 hours. Finally in step 918, the encapsulant is inspected, and the chips electrically tested, and any required rework of the chips is completed.

FIG. 13 illustrates the process 1000 for manufacturing and attaching heat sink plates 416, 418, 420 to the circuit board as shown in FIG.s 6, and for mounting and encapsulating wirebond chips 418, as shown in FIG.s 8. FIG. 14 schematically illustrates a cross section of some of the connections between the heat sink 416, flexible circuit board 400, SMT module 940, flip chip 942, and wirebond chip 944. In step 1002, cavities 946, 948 are milled in a first surface 950 of heat sink plate 416 to conform to chips mounted on the front of the circuit board, when the heat sink plate is mounted on the front surface of the circuit board as shown in FIG. 14. A measured amount of a thermally conductive paste 952 such as thermal grease or preferably, thermally conductive adhesive, such as a thermoset or thermoplastic precursor filled with metal particles, is dispensed into the heat sink cavities or onto the chips that fit into the conforming cavities.

In lay-up step 1006, heat sink surface 950 is covered with adhesive 954, and the front side 956 of circuit board 416 is positioned on the adhesive on the heat sink with heat and pressure. Preferably, the adhesive is a film adhesive, more preferably ROGERS 8970®, and preferably, the heat is at about 165-185 degrees C and the pressure is about 6.895 x 10^5 N/m^2 about 100 psi and is applied for about one second to form a connected structure. The circuit board is laminated to the heat sink with heat and pressure in step 1008. Preferably, the lamination heat is at about 130-140 degrees C for about 1 hour and at about 170-180 degrees C for 1 hour. A film adhesive 958 is placed on the adhesive layer 954 or more preferably adhesive layer 954 does not extend into the area of the window 960 formed through the circuit board so that the film adhesive 958 is placed directly on heat sink surface 950 at the window 960 and wirebond chip 944 is bonded in the window in step 1010. Preferably the film adhesive used to bond the chip to the heat sink is STAYSTICK® film. Bond wires 962, 964 are bonded to pads 966, 968 on chip 944 and pads 970, 972 on back side 974 of circuit board 400 for electrical interconnection in step 1012. Preferably, the wire is 25.4 μm (1.0 mil) thick Al-Si wire. Inspect, test and rework wirebond connections as required in step 1014. Preferably use microscopic inspection and perform a pull test on the wires and if wires pull loose to rebond the wires.

In step 1018, a ring 980, best seen in FIG. 8, is dispensed around the wirebond chip connection for encapsulating the wirebond chip, wires, and wirebond pads on the circuit board. Preferably the ring is an epoxy equal to HYSOL FP4323®. In step 1020, encapsulant 982 such as epoxy equal, is dispensed within the ring to cover the wirebond connections. Preferably, the encapsulant is HYSOL 4510®.

In step 1020, the encapsulant is gelled using heat at about 90 degrees centigrade for about 10 minutes and then at about 135 degrees centigrade for about 15 minutes. The encapsulant and wires are inspected and reworked as needed in step 1022. In step 1024, the encapsulant is cured using heat preferably in an oven at 155 degrees C for about 4 hours.

FIG. 15 illustrates the process 1050 for completing the manufacture of the cirucit board. In step 1052, PIH connectors (not shown) are positioned in

plated-through-holes (PTHs) in more flexible areas near the edge of the circuit board, and in step 1054, the pins are soldered in the PTH's preferably using a no-clean solder wire. Finally, in step 1030, the circuit board is extensively electrically tested, preferably using a probe tester.

FIG. 16 illustrates the three dimensional arrangement 1100 of the flexible circuit board 1070 and heat spreaders 1072, 1074 and 1076 in an enclosure of the preferred embodiment of the present invention. Heat spreaders 1072 and 1074 are connected together with screws 1102, 1104, best seen in FIG. 17. Screws 1106, 1108 attach the connected pair of heat spreaders 1072, 1074 to heat spreader extension 1110 and chassis or machine frame 1112 providing a thermal conduction path out of the enclosure. Screws 1114, 1116 connect heat spreader 1076 to upright heat spreader extension 1110. Other known fasteners could be substituted for the screws. In order to minimize vibration a thermally conductive adhesive with vibration, absorbing qualities may be placed between joints where heat sinks and the frame meet before connection.

Claims

1. An interconnect structure comprising:
   a flexible circuit board comprising:
   a layer of patterned copper;
   an external dielectric layer with windows through the dielectric layer; and
   contact means at the windows for electrically connecting leads or pins to the patterned copper;
   one or more electronic components on the external dielectric layer, mechanically connected to the flexible circuit board, with leads electrically connected to the connection means, and with a top surface facing away from the flexible circuit board;
   a flat heat spreader plate laminated to a portion of the external dielectric layer with at least one cavity extending from the dielectric bottom to a cavity bottom and enclosing at least one of the components; and
   heat conduction means extending between the bottom of the cavity and the top surface of the component enclosed in the cavity and the bottom of the cavity.

2. A flexible substrate for a circuit board, comprising:
   one or more flexible wiring layers of conductive metal;
   one or more flexible, dielectric layers including one separating any respective adjacent pair of the wiring layers and forming connected layers;
   means including one or more additional flexible metal wiring layers attached on only selected parts of one or more major exterior surfaces of the substrate to define thicker, stiffer areas of more complex circuitry with such additional layers and to define more flexible bend areas without such additional layers for bending the circuit board through only the flexible areas about a line;
   one or more metal heat spreader plates attached to the thicker sections; and
   conductive vias connecting between the wiring layers in the stiffer areas.

3. The substrate of claim 2 which is bent with a smaller radius at bend areas than in the functional islands.

4. The substrate of claim 2 or 3 in which the dielectric layers include polyimide film.

5. The substrate of claim 4 in which the polyimide film is about 0.025 mm thick.

6. The substrate of any one of claims 2 to 5 in which the dielectric layers are laminated to the wiring layers using an adhesive, preferably a film adhesive approximately 0.025 mm thick.

7. The substrate of any one of claims 2 to 6 in which metal wiring layers include copper foil of uniform thickness patterned to form electrical circuits.

8. The substrate of claim 7 in which the copper foil includes a foil approximately 0.018 mm thick.

9. The substrate of any one of claims 2 to 8 in which one of the additional wiring layers on the stiffer sections of each of two major exterior surfaces of the substrate consists of chemically or electrically deposited copper, preferably including layers approximately 0.025 mm thick.

10. The substrate of any one of claims 2 to 9 in which the conductive vias include one or more via holes made through the substrate being internally plated with chemically or electrically deposited copper.

11. The substrate of claim 10 in which the via holes include holes approximately 0.025 mm in diameter and are plated with the same deposited copper layer included in an outer wiring layer on each of two major surfaces of the

substrate.

12. The substrate of any one of claims 2 to 11 further comprising an additional flexible dielectric layer for each additional wiring layer extending only on said stiffer functional islands.

13. The substrate of any one of the claims 2 to 12 in which the thicker areas include one or more arrays of electrical connections at an external dielectric layer for directly connecting a chip with a mirror image array of connection pads.

14. The substrate of any one of claims 2 to 12 in which the thicker areas include one or more rectangular windows through the thicker areas surrounded by wirebond connection pads for connecting a wirebond chip in the windows.

15. The substrate of any one of claims 2 to 14 further comprising:
a core of polyimide film about 0.025 mm thick with two major surfaces;
first layers of film adhesive about 0.025 mm thick on each on a major surface of the core;
layers of copper film about 0.018 mm thick with first major surfaces of each connected by the first adhesive layers to each major surface of the core;
second layers of film adhesive about 0.025 mm thick each on a second major surface of each copper layer;
external layers of polyimide film about 0.025 mm thick each with a major internal surface connected by the second layers of film adhesive to each second major surface of the copper layers;
holes formed through the substrate;
a layer of copper, chemically or electrically deposited in the through holes, and about 0.018 mm thick selectively on a major external surface of each external layer of polyimide film and defining thicker, stiffer areas of the substrate and more flexible, thinner areas for bending the substrate;
a layer of solder mask on an exterior major surface of each layer of deposited copper at the thicker areas;
one or more arrays of electrical connections on at least one major surface of the substrate for connecting direct connection chips; and
one or more linear rows of wirebond pads forming a rectangle about every wirebond window for connecting wirebond chips.

16. A circuit board comprising:
a flexible substrate including:
at least one flexible wiring layer; and
at least one flexible dielectric layer including a layer to separate any adjacent pairs of wiring layer and an exterior dielectric layer with windows; and
connector means at the windows in the dielectric for electrically connecting pins or leads to the wiring layer;
one or more components of a first height on the exterior dielectric layer with leads connected to the connector means;
one or more components of a second, greater height on the exterior dielectric layer with leads connected to connector means.

17. The circuit board of claim 16 in which the connection array of a chip is soldered to a connection array of the substrate, preferably by soldered flip chip interconnections.

18. The circuit board of claim 16 or 17 in which the connection between a chip and the substrate is encapsulated with electrically nonconductive plastic.

19. The circuit board of any one of claims 16 to 18 in which the heat sink includes an aluminum plate.

20. The circuit board of any one of claims 16 to 19 further comprising:
one or more rectangular windows extending through the substrate at a heat sink;
wirebond pads in rectangular rows encircle the windows on the surface of the substrate opposite from the heat sink;
a chip with wirebond pads on a first major surface and positioned in the window with a second major surface of the chip bonded to the heat sink;
bonded wires connecting between respective wirebond pads of the chip and substrate; and
a plastic encapsulant encapsulating the bonded wires, wirebond pads on the substrate and the wirebond chip.

21. A circuit board comprising:
a flexible substrate including:
multiple wiring layers;
multiple dielectric layers including a layer to separate each adjacent pair of wiring layer and an exterior dielectric layer on a first major surface of the substrate;
a rectangular window extending through the substrate; and
wirebond pads in a rectangular row encircling the window on a second major surface of the substrate opposite the first major surface;
a heat sink with a first major surface laminated

to a part of the first major surface of the substrate at the window;
a wirebond chip extending through the window with a first major surface adhesively attached to the first major surface of the heat sink and with wirebond pads on a second major surface of the chip opposite to the first major surface of the chip;
wires connecting between wirebond pads of the chip and substrate; and
plastic encapsulant covering the wires, wirebond pads of the substrate and second major surface of the chip.

22. The circuit board of claim 21 in which an adhesive between the wirebond chip and the heat sink is a thermally conductive plastic.

23. A circuit board, comprising:
a substrate including:
multiple flexible wiring layers of conductive metal;
one or more flexible dielectric layers including one separating each adjacent pair of the wiring layers forming a substrate of connected layers;
one or more additional flexible metal wiring layers attached on only selected parts of one or more major exterior surfaces of the substrate and which define thicker, stiffer areas of more complex circuitry with such additional layers and define more flexible bend areas without such additional layers through which the circuit board can be bent about a line;
conductive vias connecting between wiring layers in the stiffer areas; and
one or more additional flexible dielectric layers attached on only the thicker stiffer areas;
components connected to each of the thicker, stiffer areas of the substrate;
two heat sink plates each with a first major surface attached on a first surface of the substrate to each of two adjacent thicker, stiffer areas of the substrate separated by a bend area for allowing the substrate to bend to move the heat sink plates together with a second major surface of each heat sink plate in adjacent confronting position;
means for connecting the heat sinks together to form a single structure with a second major surface of each heat sink plate in adjacent confronting position; and
means for attaching the heat sink structure to a frame for conducting heat out of the heat sink structure.

24. The circuit board of claim 23 in which means for connecting the heat sinks together include:
a first heat sink plate has one or more threaded holes in one edge; and
a second heat sink plate which includes:
an edge flange with respective through holes through which screws can be inserted to screw into the threaded holes of the first heat sink to connect the heat sinks together; and
one or more threaded holes in one edge for connection to perpendicular frame member.

25. A flexible substrate for a circuit board, comprising:
a lamellar structure with multiple flexible metal wiring layers and multiple flexible dielectric layers including a dielectric layer between each adjacent wiring layer;
via holes through the substrate in parts selected to be thicker, stiffer areas;
metal plating the through holes and forming one or more additional flexible metal wiring layers only on selected parts of the major exterior of the substrate which define thicker, stiffer areas of more complex circuitry with such additional layers and more flexible bend areas without such additional layers and through which the substrate can be bent about a line; and
a metal heat spreader plate attached to one of the thicker, stiffer areas.

26. The substrate of claim 25 in which the lamellar structure further comprises:
a layer of film adhesive positioned between adjacent metal wiring and dielectric layers.

27. The substrate of claim 25 or 26 further comprising one or more additional dielectric layers deposited only on the thicker, stiffer areas of the substrate.

28. The substrate of any one of claims 25 to 27, further comprising copper foils patterned to produce the wiring layers.

29. The substrate of any one of claims 25 to 28, further comprising rectangular windows through the substrate and in which the additional wiring layers include an external wiring layer with wirebond pads in rectangular lines about the windows.

30. A flexible circuit board, comprising:
a flexible circuit board substrate with multiple wiring layers and windows through the circuit board with wirebond connection pads near the window; and
a heat sink plate laminated to the circuit board at the windows;
wirebond chips positioned in the windows and

bonded onto the heat sink plate;
bonding wires extending between pads on the wirebond chip and wirebond pads on the circuit board at the window; and
encapsulant enclosing the wirebond chip bonding wires, and wirebond pads with an organic material.

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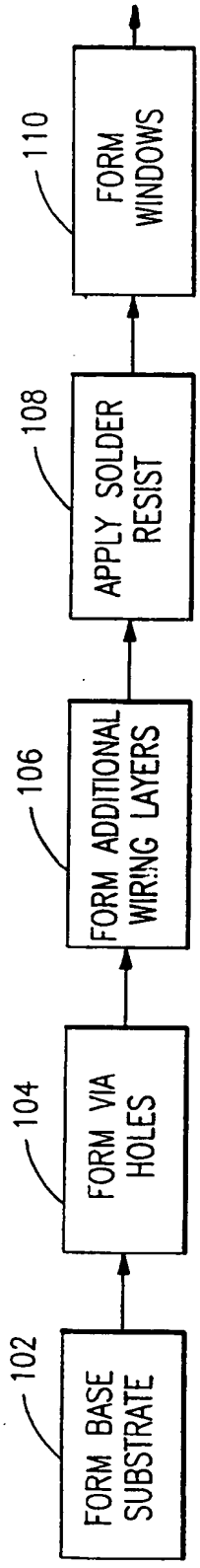

FIG.1

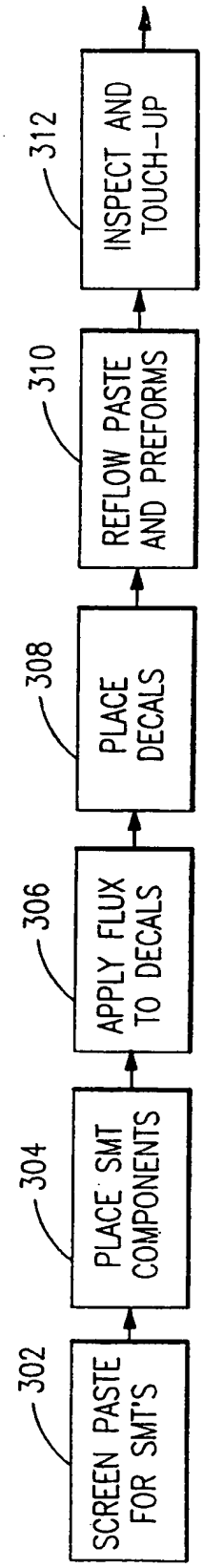

FIG.4

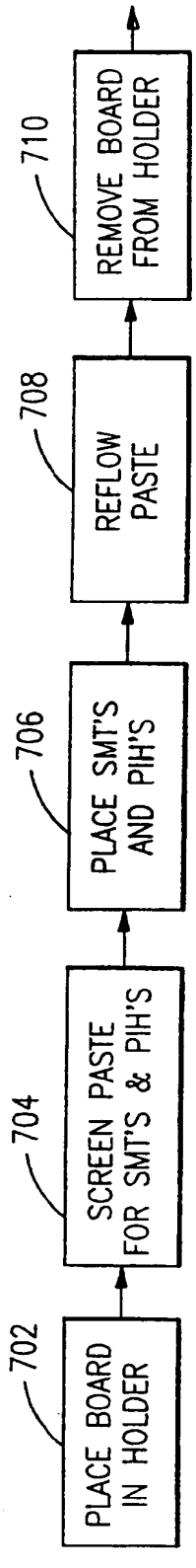

FIG.11

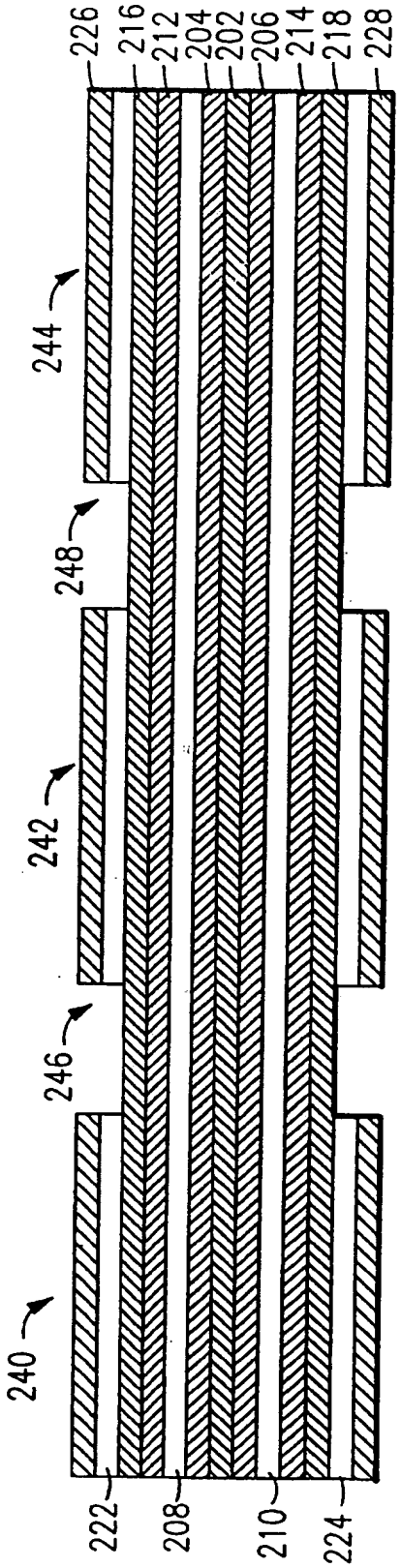

FIG.2

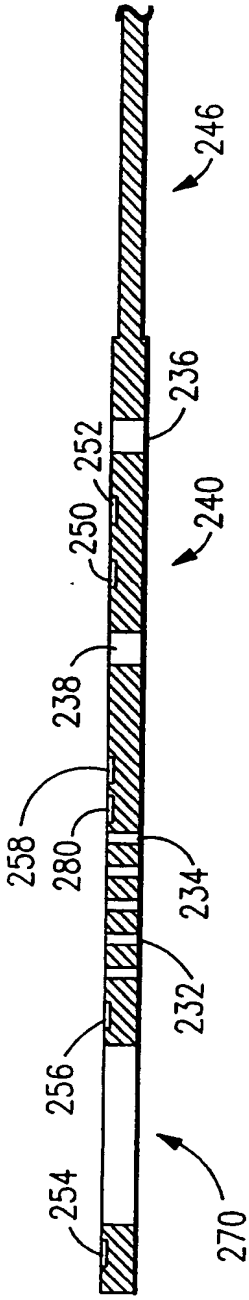

FIG.3

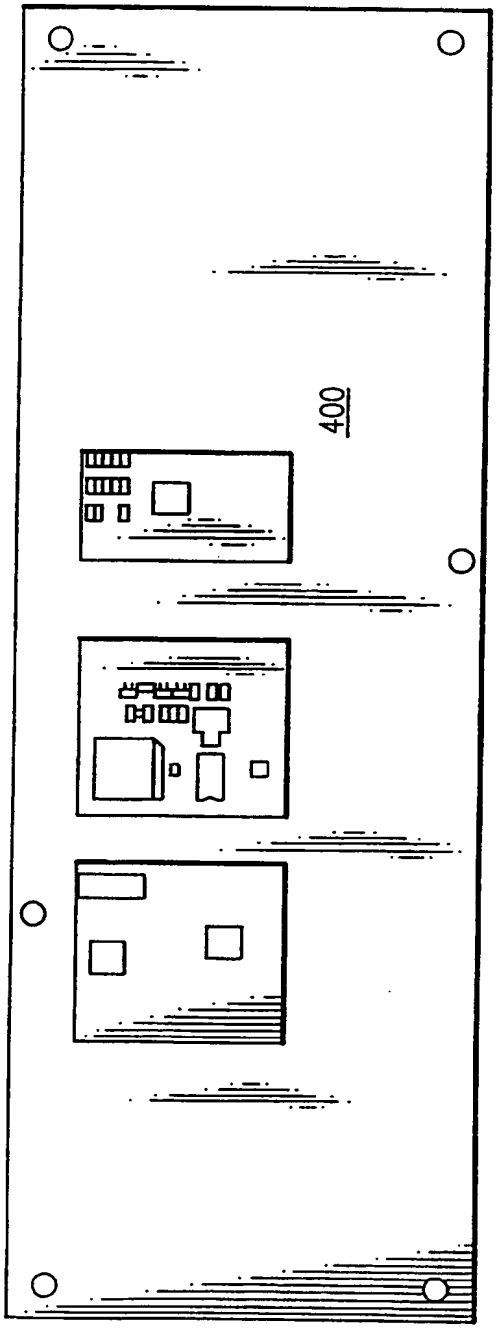

FIG.5

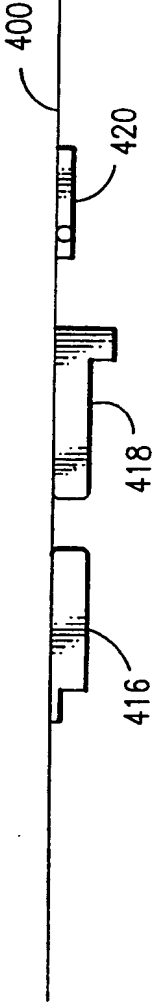

FIG.6

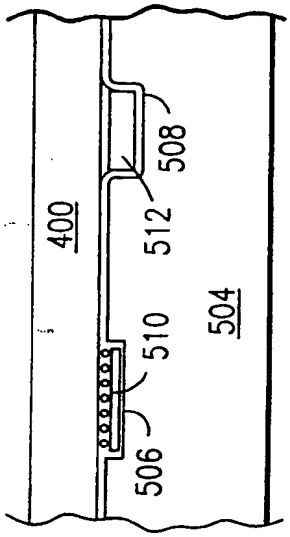

FIG.10

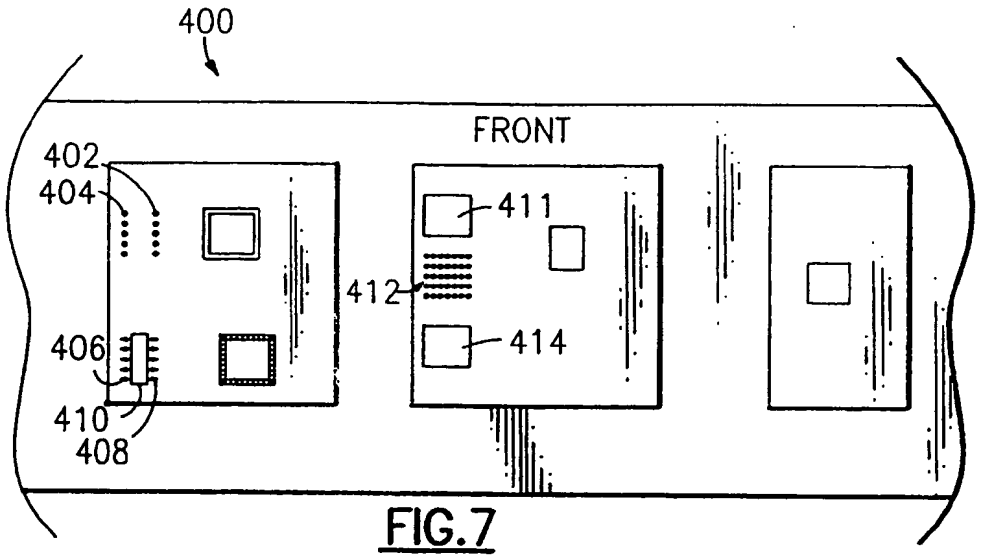

FIG.7

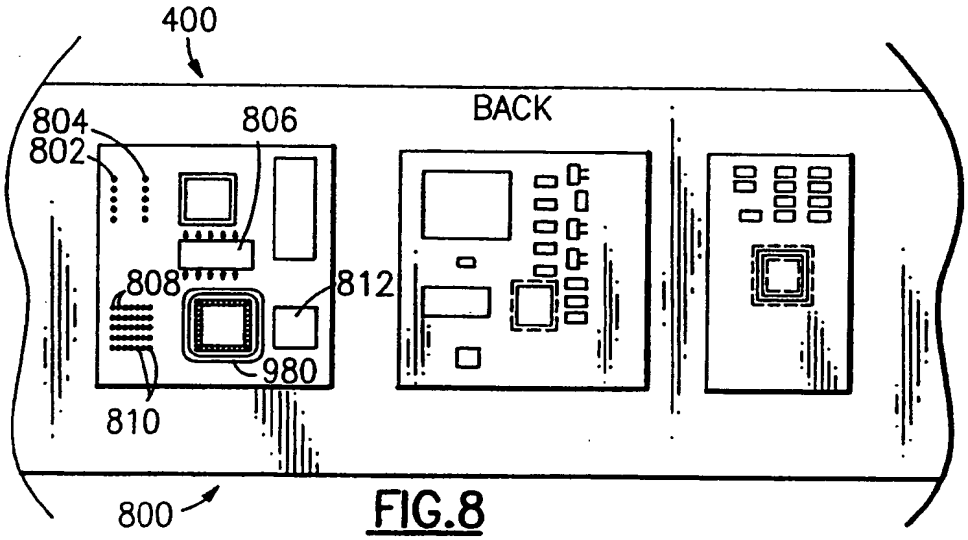

FIG.8

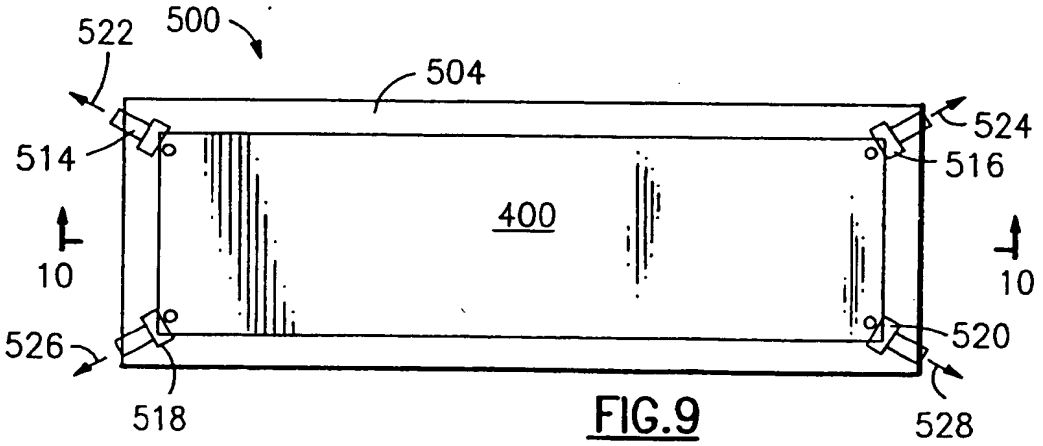

FIG.9

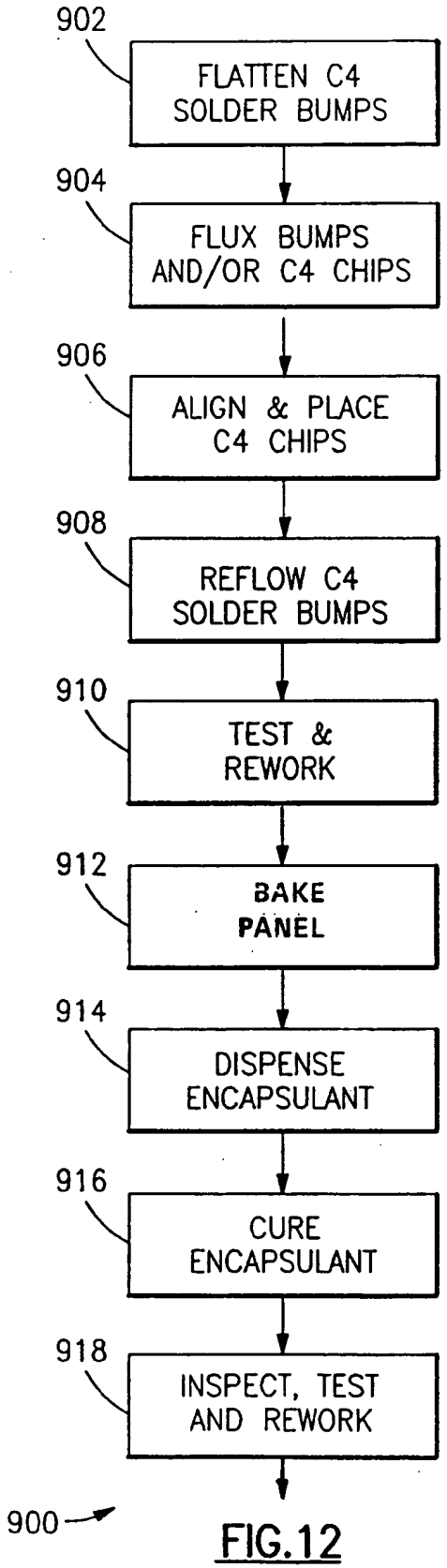

FIG.12

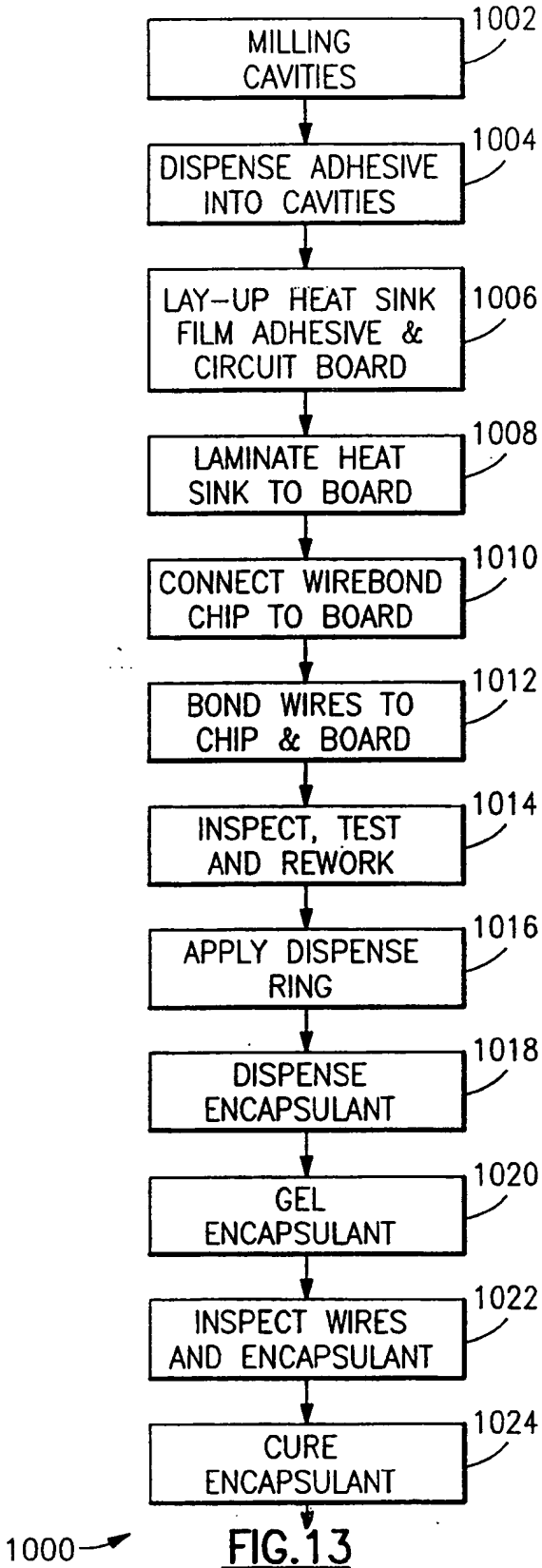

FIG.13

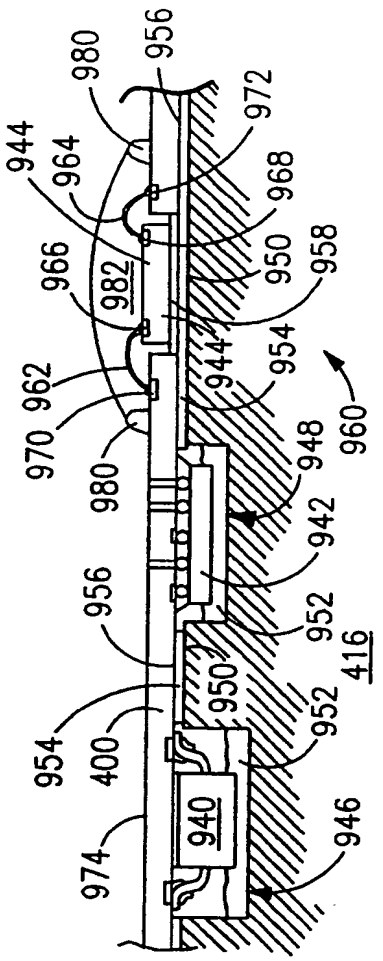

FIG.14

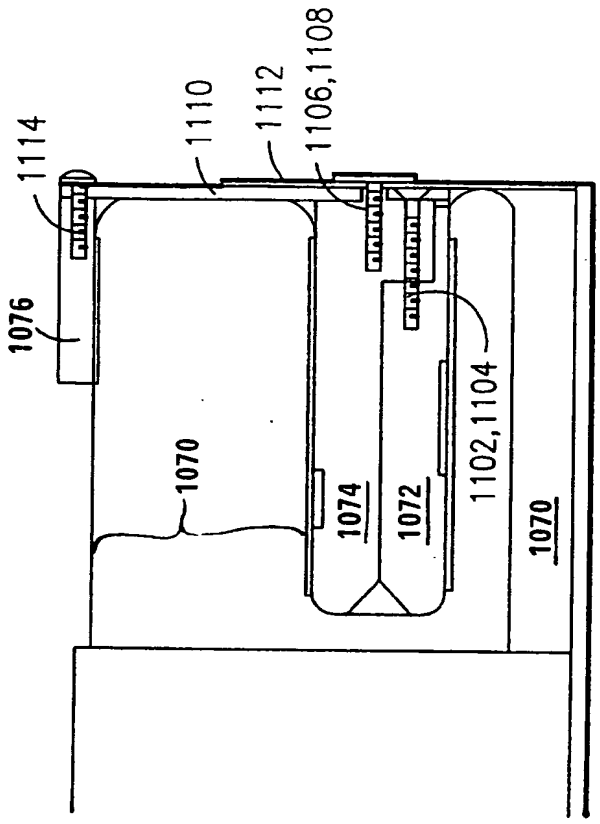

FIG.16

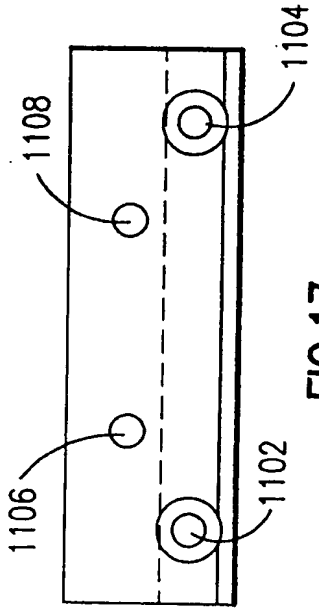

FIG.17

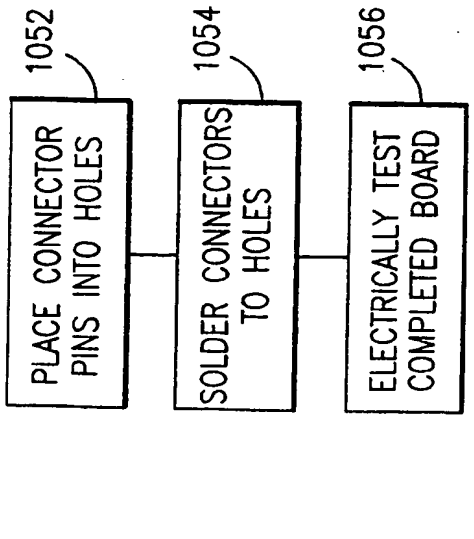

FIG.15

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 632 685 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **94108592.0**

(51) Int. Cl.[6]: **H05K 7/20**, H05K 1/00

(22) Date of filing: **01.06.94**

(30) Priority: **03.06.93 US 71630**

(43) Date of publication of application:
04.01.95 Bulletin 95/01

(84) Designated Contracting States:
DE FR GB

(88) Date of deferred publication of the search report:
17.05.95 Bulletin 95/20

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IBM Deutschland Informationssysteme GmbH
Patentwesen und Urheberrecht
D-70548 Stuttgart (DE)

(54) Flexible circuit board assembly with common heat spreader and method of manufacture.

(57) Disclosed are multi-layer substrates for flexible circuit boards and flexible circuit board assemblies and their methods of manufacture.

More particularly multi-layer flexible circuit board substrates are described for attaching components including chips and heat spreaders to form a three-dimensional circuit board assembly.

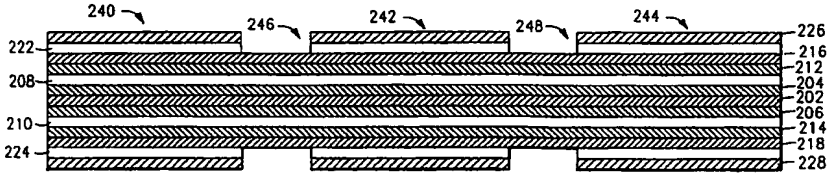

FIG.2

EP 0 632 685 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

DOCUMENTS CONSIDERED TO BE RELEVANT

EP 94108592.0

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	US - A - 4 858 073 (GREGORY) * Fig. 1-6,19-21; abstract; column 6, lines 39-54; column 9, lines 34-51; column 10, lines 30-41 *	1,2,4, 7,9, 10,16, 23	H 05 K 7/20 H 05 K 1/00
A	* Figs; abstract; claims *	3,5, 6,8, 11-15, 17-22, 24-30	
Y	US - A - 4 682 270 (WHITEHEAD) * Fig. 1-5; column 6, lines 56-64; column 7, line 51 - column 8, line 14 *	1,2,4, 7,9, 10,16, 23	
A	* Figs; abstract; claims *	3,5, 6,8, 11-15, 17-22, 24-30	
A	US - A - 4 682 269 (PITASI) * Fig. 1; abstract; column 1, line 66 - - column 2, line 9; claim 1 *	1,2,4, 7,9, 10,16, 19,23	
A	EP - A - 0 369 919 (IBM) * Fig. 1,2; abstract; column 3, line 52 - - column 5, line 32 *	1,2,4, 7,9, 10,16, 23,25, 30	
P,A	US - A - 5 261 593 (CASSON) * Figs; abstract;	16,17	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 05 K 3/00
H 05 K 1/00
H 05 K 7/00
H 01 B 17/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	27-02-1995	WENNINGER

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 94108592.0

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
	column 4, line 41 - - column 5, line 7 * --		
A	FR - A - 2 480 488 (EATON) * Fig. 5-8; page 5, line 37 - page 6, line 35 * ----	1,2,4, 7,9, 10,16, 23,25, 30	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)

The present search report has been drawn up for all claims

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)